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SUBSTITUTE FORM PTO-1449 (MODIFIED)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IBM/174DV1	SERIAL NO. 10/662,080 ~~FILED HEREWITH~~
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))		APPLICANT John Michael Borkenhagen et al.	
		FILING DATE September 12, 2003	GROUP 2824

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A.A	6 1 4 7 9 2 7	11/14/2000	Ooishi	365	233	6/3/1999
	A.B	6 2 1 9 7 4 6	4/17/2001	Vogley	711	104	12/6/1999
	A.C	6 3 1 6 9 8 0	11/13/2001	Vogt et al.	327	273	6/30/2000
	A.D	6 4 5 6 5 4 4	9/24/2002	Zumkehr	365	193	3/30/2001
	A.E						
	A.F						
	A.G						
	A.H						
	A.I						
	A.J						
	A.K						

FOREIGN PATENTS OR PUBLISHED FOREIGN PATENT APPLICATIONS

		DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION (YES/NO)
	A.L						
	A.M						
	A.N						
	A.O						
	A.P						
	A.Q						

OTHER DOCUMENTS (Including Author, Title, Date, Place of Publication)

	A.R	"Double Data Rate (DDR) SDRAM Specification", JEDEC Standard, JESD79, JEDEC Solid State Technology Association 2000, Arlington, VA, (6/2000).
	A.S	U.S. Patent Application Serial No. 09/617,558, entitled "Programmable Compensated Delay for DDR SDRAM Interface," filed on 7/17/2000 by Borkenhagen et al. (ROC920000157US1).
	A.T	

EXAMINER	DATE CONSIDERED
Tuan T. Nguyen	4/27/05

EXAMINER: Initial if citation considered, whether or not in conformance. Draw line through citation only if not in conformance and not considered. Include a copy of this form with next communication to applicant.